SILICON CARBIDE SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001] The present invention relates to a silicon carbide semiconductor device used as a power semiconductor device.

BACKGROUND ART

[0002] As already known, an IGBT or a vertical MOSFET (There are cases in which a MOS structure is a planar type or a trench type.), which is a typical example of a power semiconductor device (power device) having a MOS structure, is used, for example, as a switching element in an inverter circuit. This type of power device has a very thin gate insulating film as compared with a field oxide film or the like.

[0003] Here, a vertical power MOSFET described in Patent Document 1 is a device using Si as a semiconductor substrate material. As illustrated in FIGS. 1 and 2 in Patent Document 1, in an adjacent region on a side of a cell region of a MOSFET adjacent to a periphery of the cell region of the MOSFET (including a gate pad), minute diodes are arranged at least in one row along the periphery. Each of such diodes arranged in one row in the region between the gate pad and the cell region of the MOSFET absorbs holes that are injected from a P-well and a P-base into an N-type semiconductor layer on a drain side upon applying a forward bias when the MOSFET is switched from an ON state to an OFF state as illustrated in FIG. 3 of Patent Document 1. For this reason, the structure described in Patent Document 1 can prevent a parasitic transistor illustrated in FIG. 3 of Patent Document 1 from turning on when the MOSFET is switched from a forward bias to a reverse bias. In addition, in the structure described in Patent Document 1, the P-base which is the P-well of a MOSFET cell is electrically connected to a source electrode through a back gate as illustrated in FIG. 2 of Patent Document 2.

PRIOR ART DOCUMENT

Patent Document

[0004] Patent Document 1: Japanese Patent Application Laid-Open No. 05-198816 (1993) (FIGS. 1 to 3)

SUMMARY OF THE INVENTION

Problem to be Solved by the Invention

[0005] The problem to be solved by the present invention will be described below with reference to FIG. 2 of Patent Document 1.

[0006] Now, when a MOSFET cell which is a switching element switches from an ON state to an OFF state, a drain voltage of the MOSFET cell, that is, a voltage of a drain electrode, rapidly increases and changes from about 0 volt to several hundred volts. Then, a displacement current flows into a P-well through a parasitic capacitance present between the P-well and an N-type drain layer. As described below, although this displacement current flows into the source electrode, this is the same for the case in which the P-well that forms the parasitic capacitance between itself and the N-type drain layer is a P-well of the MOSFET cell, a P-well of a diode cell, or a P-well located below a gate pad or below a gate finger mechanically connected to the gate pad.

[0007] Here, it should be noted that, when an area of a transverse plane of the P-well of the MOSFET cell is compared with an area of a transverse plane of the P-well of the diode cell, the area of the transverse plane of the P-well below the gate pad or below the gate finger is very large. Consequently, an electric resistance value in the P-well below the gate pad or below the gate finger becomes a very large value as compared with an electric resistance value of the P-well of the MOSFET cell and an electric resistance value of the P-well of the diode cell.

[0008] In Patent Document 1, since the source electrode and a field plate illustrated in a longitudinal sectional view in a section (C) of FIG. 2 are electrically connected to each other, the displacement current flowed into the P-well below the gate pad or below the gate finger during switching flows, inside the P-well below the gate pad or below the gate finger, from a portion on a side of the MOSFET cell toward a portion of a contact hole connected to the field plate, and flows into the source electrode through the field plate.

[0009] As described above, the area of the transverse plane of the P-well below the gate pad or below the gate finger is very large as compared with the areas of the transverse planes of other P-wells. However, since resistances are present in the P-well itself and the contact hole, when the displacement current flows in the P-well having a large area of the transverse plane and located below the gate pad or below the gate finger, a potential drop of a value that cannot be ignored is generated in the P-well.

[0010] As a result of this, a portion having a large distance in a horizontal direction from a portion (a portion immediately below the contact hole) which is electrically connected to the source electrode through the contact hole and the field plate in the P-well has a relatively large potential. Additionally, this potential becomes larger as a fluctuation of a drain voltage V relative to a time t, that is, dV/dt, becomes larger.

[0011] For this reason, as illustrated in the section (C) of FIG. 2 of Patent Document 1, in the case where the gate electrode is provided, through a gate insulating film, in a portion of a side edge of the cell that is farthest from the contact hole in the P-well below the gate finger connected to the gate pad, an electric field having a large strength is applied to a gate insulating film between the gate electrode having a voltage value close to 0 volt in a state immediately after the MOSFET cell is switched from an ON state to an OFF state and the portion of the side edge of the cell of the P-well. This sometimes causes a breakdown of an electrical insulation of the gate insulating film.

[0012] Therefore, recently, it has been expected to reduce a loss in an inverter circuit by using, as an switching element of an inverter circuit, a SiC semiconductor device (for example, vertical MOSFET or IGBT) using, as a semiconductor substrate material, silicon carbide (SiC) having a band gap which is three times larger than that of Si used as a conventional semiconductor substrate material. In addition, a further high-speed driving of the switching element is demanded to achieve a further low loss. To state it differently, it is demanded to further quicken the fluctuation dV/dt of the drain voltage V relative to the time t to achieve a lower loss.

[0013] The structural problem that is pointed out with reference to Patent Document 1 is a problem that may be caused similarly even if Si as a conventional semiconductor substrate material is replaced with SiC described above. Furthermore, in the case where the semiconductor substrate material is SiC, it is demanded to further quicken the fluctuation dV/dt of the drain voltage V relative to the time t as described above. As a